Vidyavardhini's College of Engineering & Technology, Vasai

Department of Computer Engineering

Academic Year 2020-21

Sub: Microprocessor (CSC501)

Year/Sem:- TE/ Sem V
Max. Marks: 50

Q.No.	Questions	Marks
1	The size of each segment in 8086 is: a)64KB b)24KB c)50KB d)16KB	2
2	Which register containing the 8086/8088 flag ? a) Status register b) Stack register c)Flag register d) Stand register	2
3	The pin configuration of 8086 is available in the_____: a)40 pin b)50 pin c)30 pin d)20 pin	2
4	The BIU contains FIFO register of size____ bytes a)8 b)6 c)4 d)12	2
5	Which of the following instruction is not valid? a) MOV AX, BX b) MOV DS, 5000H c) MOV AX, 5000H d) PUSH AX	2
6	The instructions that involve various string manipulation operations are a) branch instructions b) flag manipulation instructions	2

	c) shift and rotate instructions d) string instructions	
7	The instruction that pushes the contents of the specified register/memory location on to the stack is a) PUSHF b) POPF c) PUSH d) POP	2
8	The instructions that are used for reading an input port and writing an output port respectively are a) MOV, XCHG b) MOV, IN c) IN, MOV d) IN, OUT	2
9	The instruction that is used for finding out the codes in case of code conversion problems is a) XCHG b) XLAT c) XOR d) JCXZ	2
10	The instruction that pushes the flag register on to the stack is a) PUSH b) POP c) PUSHF d) POPF	2
11	The type of the interrupt may be passed to the interrupt structure of CPU from a) interrupt service routine b) stack c) interrupt controller d) interrupt non controller	2
12	At the end of ISR, the instruction should be a) END b) ENDS c) IRET d) INTR	2
13	After every response to the single step interrupt the flag that is cleared is a) IF (Interrupt Flag) b) TF (Trap Flag) c) OF (Overflow Flag) d) None of the mentioned	2
14	Port C of 8255 can function independently as a) input port	2

	b) output port c) either input or output ports d) both input and output ports	
15	If A1=0, A0=1 then the input read cycle is performed from a) port A to data bus b) port B to data bus c) port C to data bus d) CWR to data bus	2
16	The pin that clears the control word register of 8255 when enabled is a) CLEAR b) SET c) RESET d) CLK	2
17	In control word register, if SC1=0 and SC0=1, then the counter selected is a) counter 0 b) counter 1 c) counter 2 d) counter 3	2
18	In 8257 (DMA), each of the four channels has a) a pair of two 8-bit registers b) a pair of two 16-bit registers c) one 16-bit register d) one 8-bit register	2
19	In 8257 register format, the selected channel is disabled after the terminal count condition is reached when a) Auto load is set b) Auto load is reset c) TC STOP bit is reset d) TC STOP bit is set	2
20	The 80386DX has an address bus of a) 8 address lines b) 16 address lines c) 32 address lines d) 64 address lines	2
21	The number of debug registers that are available in 80386, for hardware debugging and control is a) 2 b) 4 c) 8 d) 16	2
22	80386DX is available in a grid array package of a) 64 pin	2

	b) 128 pin c) 132 pin d) 142 pin	
23	In Pentium's superscalar architecture, the number of instructions that are executed per clock cycle is a) 1 b) 2 c) 3 d) 4	2
24	The throughput of a super scalar processor is _____ a) less than 1 b) 1 c) More than 1 d) Not Known	2
25	The _____ plays a very vital role in case of super scalar processors. a) Compilers b) Motherboard c) Memory d) Peripherals	2